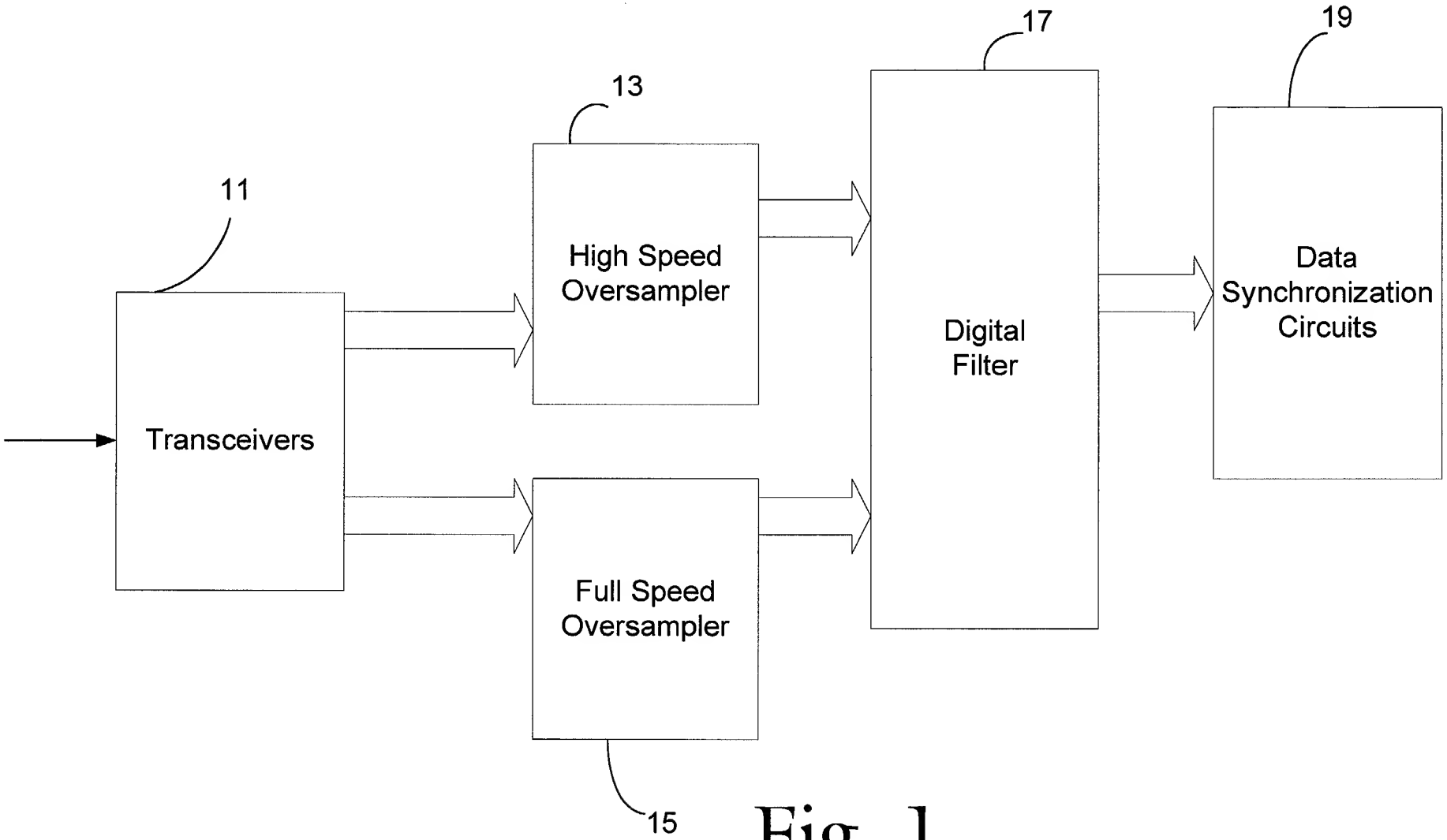
11
Transceivers
13
High Speed Oversampler
15
Full Speed Oversampler
17
Digital Filter
19
Data Synchronization Circuits

Fig. 1

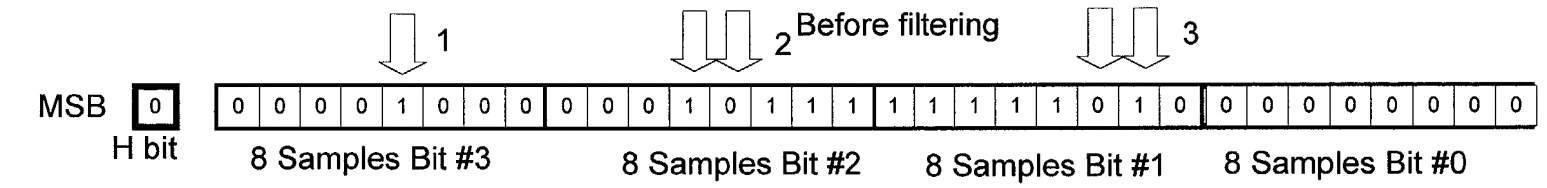

Fig. 2a

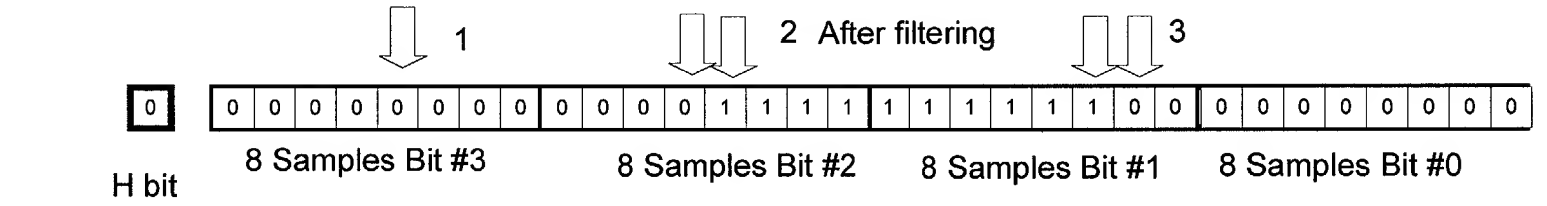

Fig. 2b

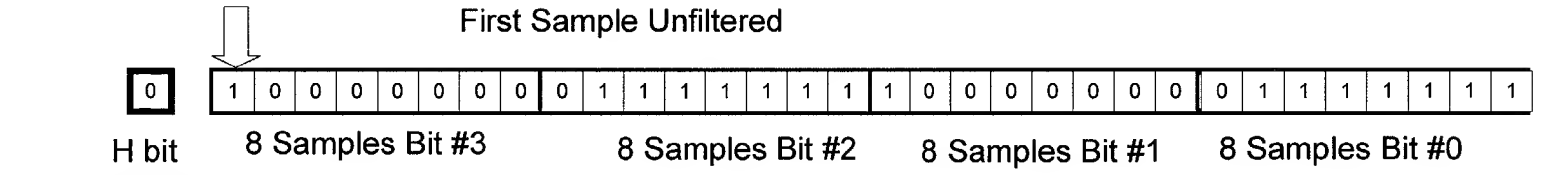

Fig. 2c

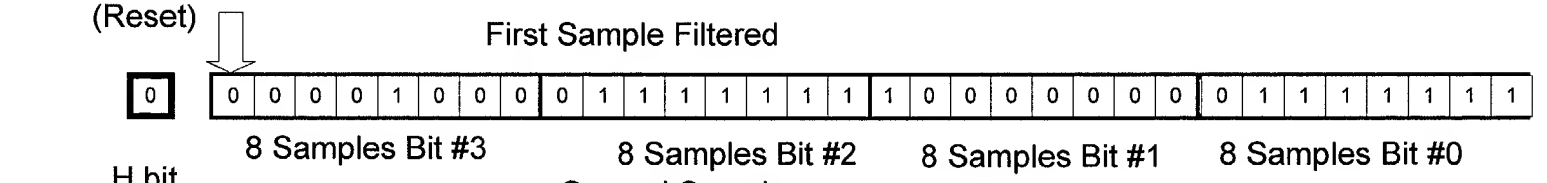

Fig. 2d

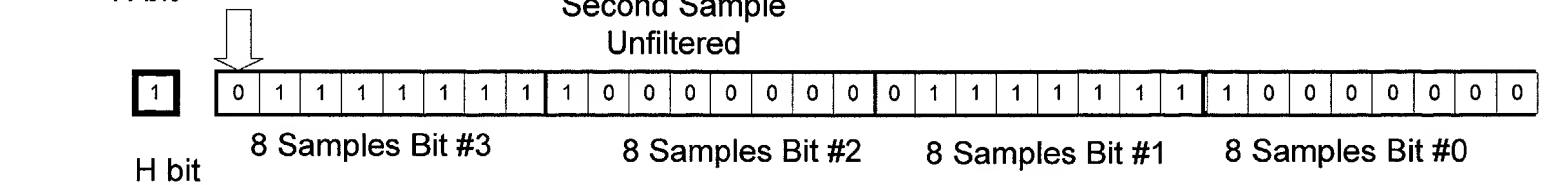

Fig. 2e

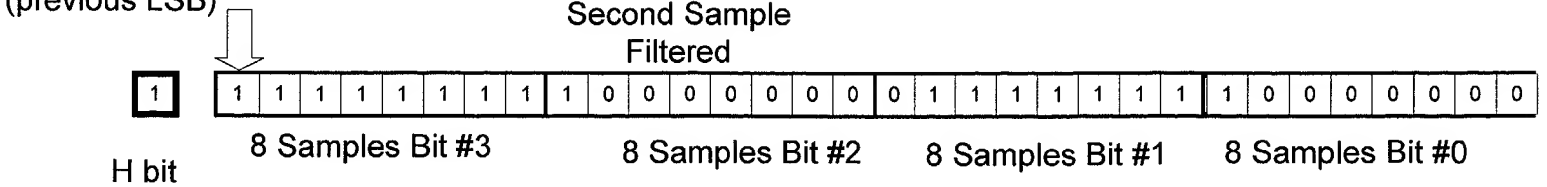

Fig. 2f

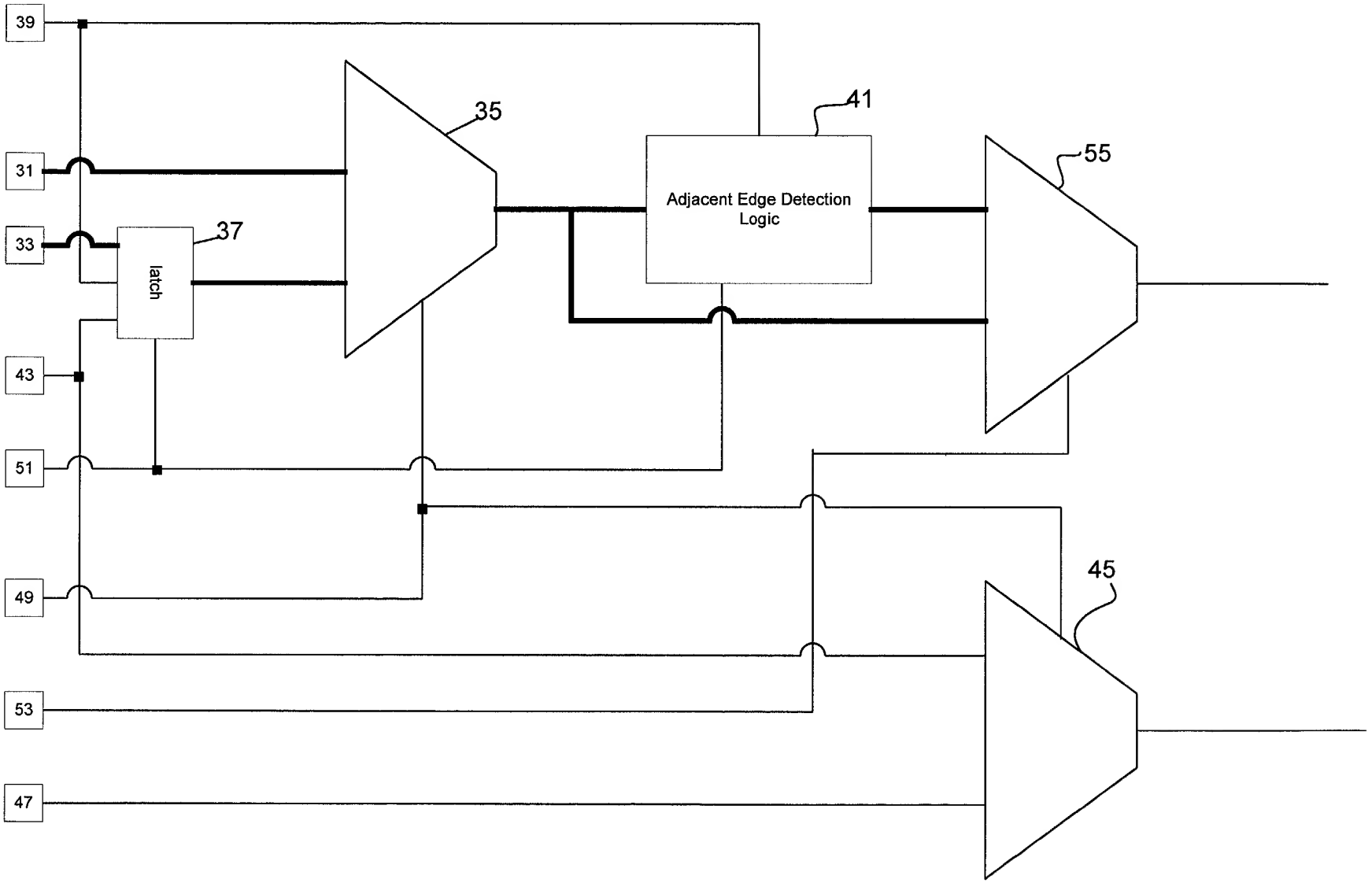
39
31
33
43
51
49
53
47
35
37
latch
41
Adjacent Edge Detection Logic
55
45

Fig. 3

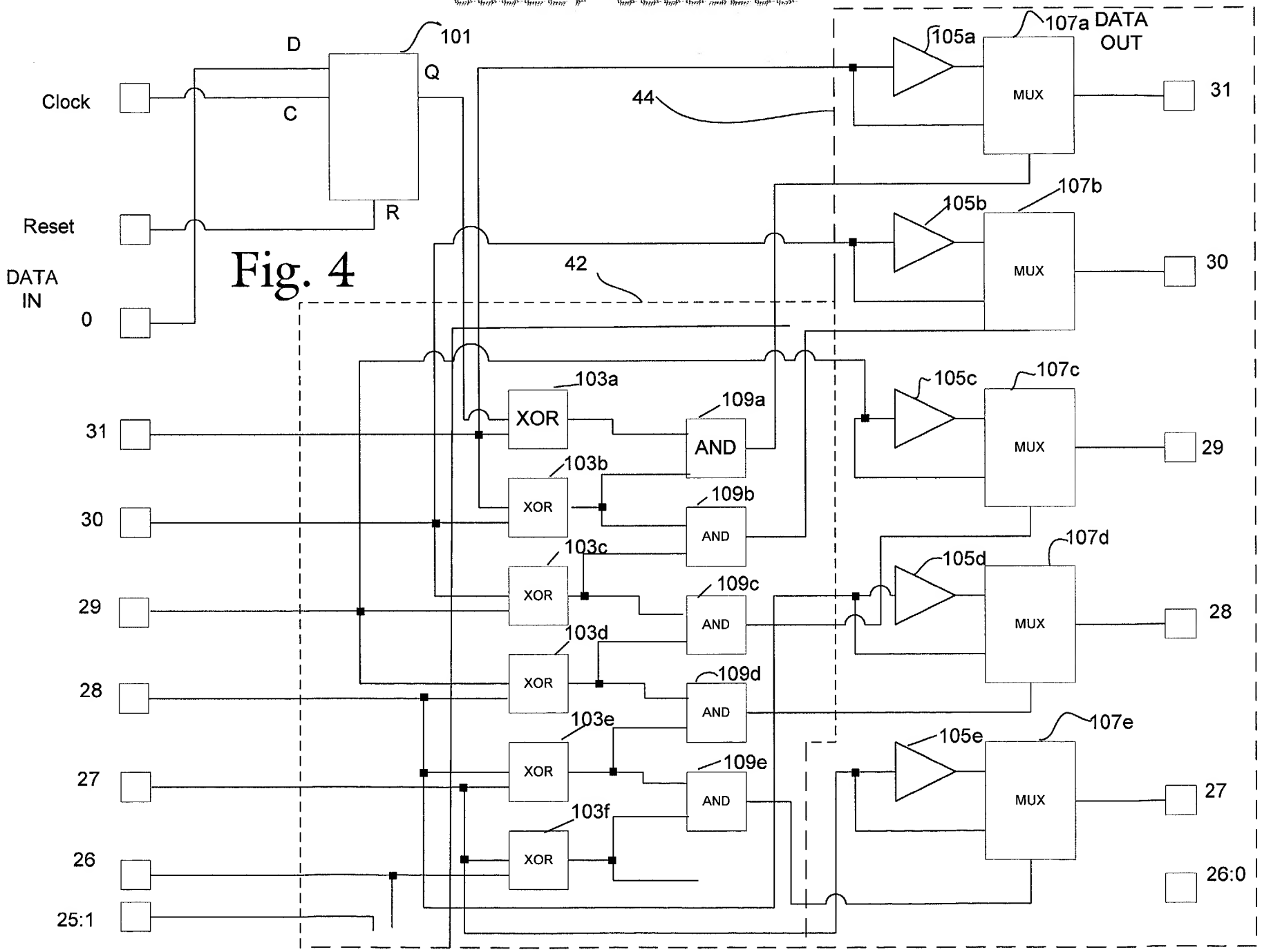
Clock
Reset
DATA IN
0
D
C
R
Q
101
44
42
DATA OUT
105a
107a
MUX
31
105b
107b
30
105c
107c
29
105d
107d
28
105e
107e
27
26:0
31
30
29
28
27
26
25:1
103a
XOR
109a
AND
103b
109b
103c
109c
103d
109d
103e
109e
103f

Fig. 4

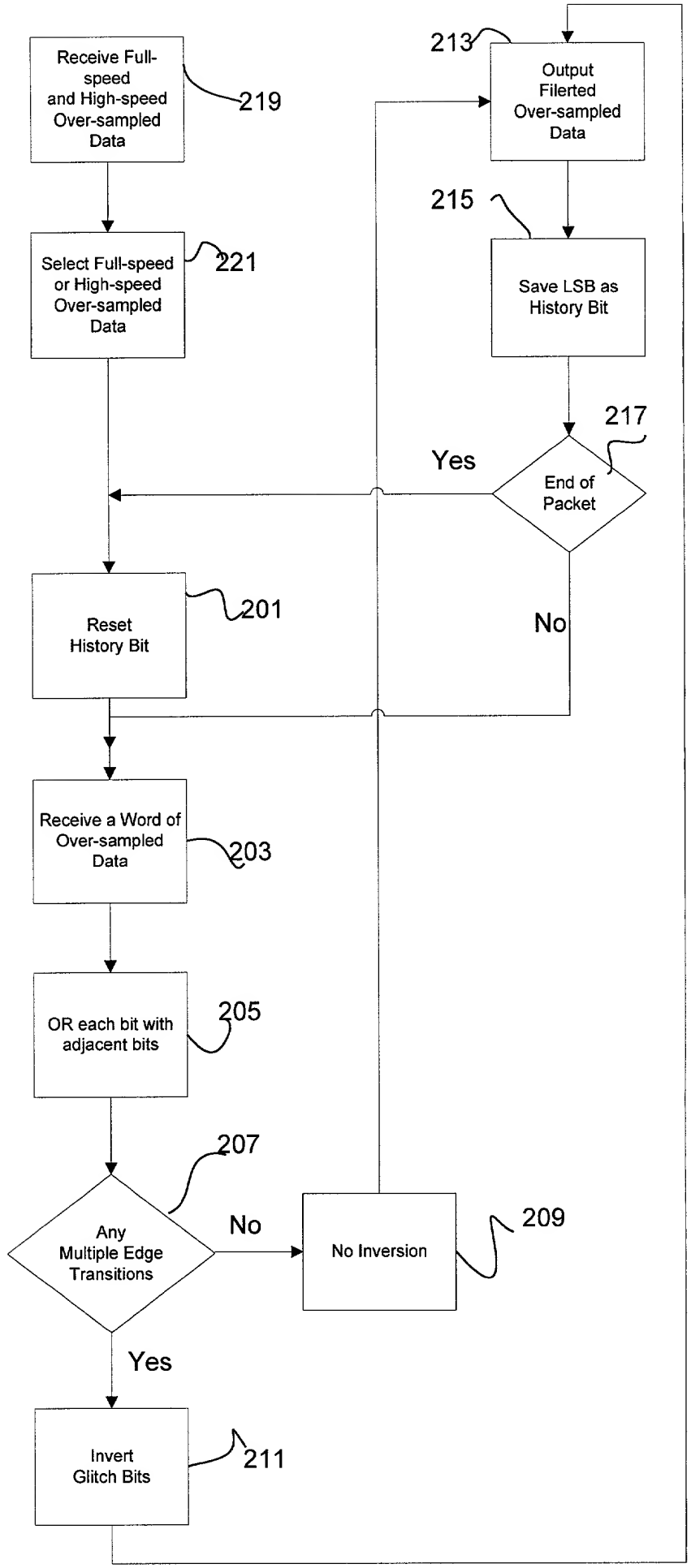
Receive Full-speed and High-speed Over-sampled Data
219
Select Full-speed or High-speed Over-sampled Data
221
Reset History Bit
201
Receive a Word of Over-sampled Data
203
OR each bit with adjacent bits
205
Any Multiple Edge Transitions
207
No
No Inversion
209
Yes
Invert Glitch Bits
211
213
Output Filerted Over-sampled Data
215
Save LSB as History Bit
217
End of Packet
Yes
No

Fig. 5